320 x 256 Complementary Barrier Infrared Detector Focal Plane Array for Long-wave Infrared Imaging

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ABSTRACT

A 320 x 256 Complementary Barrier Infrared (CBIRD) focal plane array for long-wavelength infrared (LWIR) imaging is reported. The arrays were grown by molecular beam expitaxy (MBE) with a 300 period 1.9 um thick absorber. The mean dark current density of 2.2 x 10^{-4} A/cm² was measured at an operating bias of 128 mV with a long wavelength cutoff of 8.8 µm observed at 50% of the peak. The maximum quantum efficiency was 54% measured at 5.6 µm. Operating at T = 80K, the array yielded an 81% fill factor with 97% operability. Good imagery with a mean noise equivalent different temperature (NEAT) of 18.6 mK and a mean detectivity of D* = 1.3 x 10^{11} cm-Hz^{1/2}/W was achieved. The substrate was thinned using mechanical lapping and neither an AR coating nor a passivation layer was applied. This article provides the details of the fabrication process for achieving low-dark current LWIR CBIRD arrays. Discussion for an effective hard mask for excellent pattern transfer is given and appropriate mounting techniques for good thermal contact during the dry etching process is described. The challenges and differences between etching large 200 µm test diodes and small 28 µm FPA pixels are given.

Keywords: Inductively Coupled Plasma Dry Etching, Superlattice Detectors, Long-wavelength Infrared, Focal Plane Arrays, InAs/GaSb

1. INTRODUCTION

The need for dry etching has been proven for achieving high fill-factor, small pitch focal plane arrays (FPAs). The potential impact of the dry etch process on the detector performance justifies the need for complete understanding and optimization. The importance of the etch parameters on achieving clean sidewalls, smooth surface morphology, and anisotropic etching has been reported in [1][2][3]. However, little to no discussion has been provided on additional factors that play an equally important role on the sidewall quality and device performance.

This article discusses the dry etch process for achieving low dark current LWIR CBIRD FPAs. First, the dielectric hard mask is discussed. Details on how to achieve a high, density robust mask with excellent pattern transfer is provided. Following, we converse about different methods for mounting the wafer to the carrier plate. This is needed to ensure good thermal contact during the etching to maintain a stable temperature at the material surface and also to achieve good uniformity across the wafer. Then, we compare the results of pixel delineation, using a inductively coupled plasma (ICP) dry etch system, on large sparsely, populated mesas for test detectors and small, densely packed pixels for FPAs. Etch rate, sidewall morphology, and sidewall profile were all found to differ due to the pixel spacing and amount of exposed epi-grown material. The etching process is then demonstrated on a 320×256 CBIRD FPA imaging at 80K with an $8.8 \mu m$ cutoff.

2. GROWTH, FABRICATION, AND CHARACTERIZATION

The device structure used in this work is a long-wavelength CBIRD design [4] consisting of an InAs/GaSb superlattice (SL) absorber surrounded by an InAs/AlSb hole barrier and an InAs/GaSb electron barrier. The device was grown on a 50-mm Te-doped GaSb (100) substrate in a Veeco Applied-Epi Gen III molecular beam epitaxy (MBE) chamber. The material was characterized using X-ray diffraction (XRD), surface scan, atomic force microscope (AFM), and low temperature photoluminescence (PL). The pixels of the FPA were then fully reticulated down to the bottom contact using an ICP dry etch system. Further detailed information on the etching process will be provided later in this article. Following this, Pt/Au/Ni/Au ohmic contacts were evaporated on top, and then small indium bumps were deposited over

the contacts. Arrays were individually diced and then hybridized using an FC-300 flip-chip bonder, onto a FLIR/Indigo direction injection ISC0903 ROIC. An epoxy underfill was applied, and then the substrate was completely removed by mechanically lapping, followed by a separate ICP dry etch process to finish complete removal of the substrate. The test detectors and FPA were mounted, wire-bonded, and cooled to 80K for testing and imaging. No passivation or AR coating was applied.

3. DRY ETCHING PROCESS

While techniques and approaches for the dry etching process have been detailed in various publications, external factors that indirectly affect the outcome of the pixel delineation have not been addressed. This includes the chamber condition and cleanliness, hard mask quality, wafer mounting technique, mask layout, and wafer size. Each one of these will be discussed separately below. In this work, test detectors refer to large 2µm square diodes and FPA pixels refer to small 28 µm square pixels compatible with the ISC0903 ROIC.

3.1 Chamber Condition and Cleanliness

The cleanliness and condition of the chamber during the etch process is very important, as it can contribute to unwanted effects such as re-deposition of particulates from the chamber wall. First, the DC bias is used as an indicator that the system needs to be clean. To clean the chamber, the most effective and fastest method found was to use SF₆/O₂ plasma. Following this, the chamber is opened up and wiped down with solvents. This step is necessary due to the detrimental effects fluorine has previously had on the device performance. Finally, the cleaning is completed with an overnight pumpdown and bakeout. Conditioning the chamber is done using the same exact recipe as the SL etch with the silicon carrier wafer in the chamber system and a large GaSb substrate placed on top. Figure 1 plots the dark current density, SL etch rate, and DC bias as a function of the number of hours the system has been conditioned. As can be noted, the bias continues to drop as the system becomes conditioned closer to its prime state. Once the system reaches its prime state, the bias, etch rate, and dark current density all begin to stabilize and reach ideal values. Due to limitations that the authors experienced with their individual system, the same etch process was used for chamber conditioning as was used for device fabrication, and this led to slow etch rates and consequently long conditioning times. However, this can be avoided by using a recipe with higher etch rates. Further, the plot shown represents CH₄/H₂ conditioning; significantly shorter times were experienced with BCl₃ or Cl₂ conditioning.

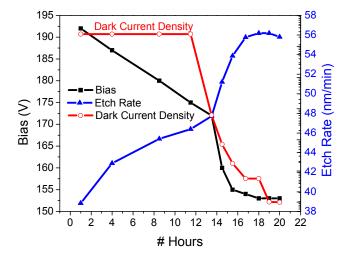


Figure 1. DC Bias, CBIRD dark current density, and SL etch rate for CH₄/H₂ conditioning of the ICP system used at JPL. Shorter conditioning times are expected for BCl₃/Cl₂ plasma.

3.2 Dielectric Hard Mask

For dry etching in the ICP system, a dielectric hard mask was required due to the heating effect the high density plasma had on photoresist. It is desired for the hard mask to undergo minimal erosion so as not to interact with the ions or byproducts during the etch process. Furthermore, achieving near-vertical sidewalls with straight edges can only be achieved with the proper pattern transfer. A poor mask with tapered sidewall profile and unwanted ripples will limit the quality of the etched pixels. To achieve these features with the hard mask, three different entities were optimized: hard mask material, deposition technique, and RIE gases for patterning.

For the dielectric hard mask, there were two different materials to choose from: SiO_2 and SiN_x . The choice was made based on the gases used during the ICP etch of the pixels, and the CBIRD structure etch recipe is primarily methane-based [1]. For methane-based etching of III-V materials, the formation of polymer during the etch has been reported [5],[6], however this effect has been found to be beneficial due to its ability to protect the sidewall from plasma-induced damage [7],[8]. Given the potential for O_2 to remove polymers and large amount of unwanted mask erosion that has been observed with SiO_2 in methane/hydrogen based plasmas[9], SiN_x was selected.

For the deposition technique, two different systems were compared: a conventional plasma enhanced chemical vapor deposition (PECVD) and an ICP-PECVD. The ICP-PECVD uses an ICP as the source, allowing for denser, higher quality films at lower deposition temperatures [10]. The differences between the systems were found to be obvious in both the erosion or loss rates during the pixel etch and also with the sharpness of the mask during pattern definition. For both SiO_2 and SiN_x , less mask waviness and sharper corners were achieved when the films were deposited by ICP-PECVD. Due to the potential degradation when exposing SL devices to high temperatures, the depositions were performed at a temperature of 150° C, and both techniques were independently optimized to achieve the highest mask density. The ICP-PECVD SiN_x appeared to have undergone less erosion during the etching of the SL pixels at a rate of 1.1 nm/min, which was 2.8 times lower than SiN_x deposited by conventional PECVD. To optimize the ICP-PECVD deposition, a higher density was achieved with lower ICP powers and also a gas flow ratio reduced to $SiH_4:N_2 = 3:4$, leading to a lower measured refractive index.

To pattern the dielectric hard mask, a simple RIE system was used and two different gas mixtures were compared. Any taper in the hard mask can subsequently limit the sidewall angle of the FPA pixels, and it was found that the gas selection played a large role in affecting this taper. Cross-sectional SEM of the same SiN_x mask etched with CF_4/O_2 and CHF_3/Ar are shown in Figure 2. For purposes of discerning the large impact, a thick 800 nm mask was deposited. A significant improvement was observed when patterning the hard mask using CHF_3/Ar , achieving a near-vertical profile with an angle of 83.2°. This is compared to 35.6°, achieved when CF_4/O_2 was used. To achieve this near-vertical profile in the CHF_3/Ar etch, the gas flow ratio was found to have the largest impact, with an optimal ratio being $CHF_3:Ar=2:3$. The result of this led to a SL sidewall improvement by at least 8°.

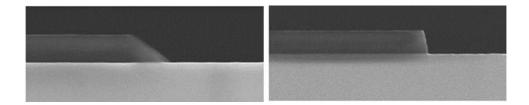


Figure 2. Cross-sectional SEM images of a 800 nm ICP-PECVD deposited SiN_x patterned using (left) CF_4/O_2 and (right) CHF_3/Ar .

3.3 Wafer Mounting Technique

For good etch uniformity and proper heat transfer, it is important that the proper wafer mounting technique is used. A good mounting technique will use a medium that can be uniformly applied, does not outgas or cause contamination in the chamber, and can be easily removed. In this work, three different media were experimented with: Apezion M high-vacuum grease, fomblin oil, and PR 220-3 photoresist. The high-vacuum grease had good thermal contact, but uniform

spreading of the grease was hard to achieve and was user dependent, leading to inconsistent results. Fomblin oil was very runny and messy to remove. Further, the oil caused issues when the sample was pumped down in the loadlock. The oil would spread out to the edge of the wafer and then on top of the sample, and any material that had been touched by the oil was then damaged. Finally, the photoresist was found to be the best choice amongst the three. The photoresist was spun onto the carrier wafer with a thickness that depended on the size of the wafer and removal post-etch was done using acetone.

3.4 Pixel Spacing and Exposed Epi-Grown Material

During the developmental stage, quick feedback and reduced optimization times are desired, and this can be done by using test detectors that are made large enough such that the detectors can easily be wire-bonded and the dicing, hybridization, underfill, backside thinning process can be avoided. However, differences in both electrical performance and mechanical characteristics were observed when the same etch process was used for the test detectors and the FPA pixels. Therefore, the optimal parameters for the test detectors will differ from the optimal parameters for the FPA pixels, so an adjustment is required. This was found to be especially true for chlorine-based etches where high volatilities may require a larger amount of adjustment. The reason for this is because the FPA pixels are more closely spaced and also there is a lesser amount of exposed epi-grown material. For this work, the large test detectors are spaced at least $100 \mu m$ apart and contain 81.7% of exposed epi-grown material, whereas the FPA pixels are spaced $2 \mu m$ apart and contain 20.7% of exposed epi-grown material.

The change in pixel spacing and amount of exposed epi-grown material had several effects. The first is the etch rate, which were found to be 14-20% lower for FPA pixels due to the reduced efficiency in both reaction removal and reactant supply. The second was with sidewall morphology. The FPA pixels were found to have more re-deposition on the sidewalls. The re-deposition not only led to more rough sidewalls, but also had an impact on the dark current of the devices. In extreme cases, the build is significant such that the sidewalls of the FPA are coated with indium droplets and the arrays appear black in color to the human eye. To alleviate this issue, a higher amount of physical etching was incorporated by increasing the byproduct removal rate relative to the reaction rates. Finally, the last difference is with the sidewall angle. For the FPA pixels, the sidewall angle became more sloped, most likely due to a higher probability for non-directionalized impinging on the sidewalls. The larger spacing with the test detectors allows for species to undergo fewer collisions and as a result a 14-20% difference in sidewall angle.

To transition from dry etching test detectors to dry etching pixels in an FPA array, the optimized etch parameters for the test detectors are initially used as the starting point. Depending on the pixel spacing and amount of exposed epi-grown material, adjustments are made to increase the amount of physical sputtering. This can be done by increasing the bias (10-25 V), adjusting the temperature (±40-60°C), and/or increasing the pressure (5-10 mTorr). Note that changing any of these parameters may negatively affect another characteristic of the etching, so the choice of which parameter to optimize should be made with taking all factors into account. For samples that were primarily dominated by physical sputtering, there was less of a difference in etch rate and a larger change in sidewall angle. As a result, the optimal etch parameters for the test detectors and FPA pixel had less of a disparity. Example cross-sectional SEMs comparing the same etching for test detectors and FPA pixels is given in Figure 3.

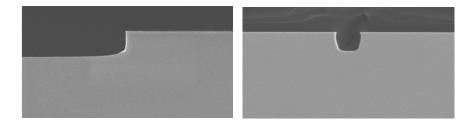


Figure 3. Cross-sectional SEM images of the same etch process used on the same CBIRD material patterned into (left) large 200 μ m test detectors spaced 100 μ m apart and (right) small 28 μ m FPA pixels spaced 2 μ m apart. SEM images were captured at a magnification of 15,000x

4. 320×256 COMPLEMENTARY BARRIER INFRARED DETECTOR FOCAL PLANE ARRAY

We apply the etching process described above to a 320×256 CBIRD LWIR FPA. The FPA is operated at 80K and an image is shown in Figure 4. The etching process achieved a fill factor of 81% and good uniformity with a 97% operability. The array was operated at a bias of 128 mV, and the measurements yielded a mean dark current of 2.2×10^{-4} A/cm² and an NE Δ T of 18.6 mK. Using 300K background illumination and f/2 optics, a mean detectivity of D* = 1.3×10^{-11} cm-Hz^{1/2}/W was obtained. Full characterization and detailed description of the FPA performance is described in Ref. [11]



Figure 4. Image taken from a 320 x 256 CBIRD LWIR FPA at T = 80K. The FPA pixels were fully reticulated using the dry etch process described in this work.

5. CONCLUSION

We demonstrated improved etching by considering factors that affect the etching process and quality of the SL FPAs. We provided our technique used to properly condition the ICP chamber and clean it to prevent any byproduct redeposition. We discussed ways to improve the dielectric hard mask quality to reduce interactions from the eroded mask material, straight pattern transfer, and prevent limitations in achieving vertical sidewalls. We further discussed how to achieve good etch uniformity with a practical mounting technique. Finally, we discuss the changes experienced when transitioning from large, sparsely populated test detectors used in the development stage to small, densely packed FPA arrays. Techniques to account for these changes, how to overcome the challenges, and the optimization process for this have been provided. Finally, the etching process is applied to a 320 × 256 CBIRD LWIR FPA.

6. ACKNOWLEDGEMENTS

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REFERENCES

[1] Jean Nguyen, Alexander Soibel, David Z.-Y. Ting, Cory J. Hill, Mike C. Lee, and Sarath D. Gunapala, "Low dark current long-wave infrared InAs/GaSb superlattice detectors", *Appl. Phys. Lett.* **97**, 051108, (2010).

- [2] Siew Li Tan, Yu Ling Goh, Sankha dip Das, Shiyong Zhang, Chee Hing Tan, John P. R. David, Nutan Gautam, Hasul Kim, Elena Plis, and Sanjay Krishna, "Dry etching and surface passivation techniques for type-II InAs/GaSb superlattice infrared detectors", *Proc. SPIE* **7838**, 783814-1, (2010).
- [3] Edward Kwei-wei Huang, Darin Hoffman, Binh-Minh Nguyen, Pierre-Yves Delaunay, and Manijeh Razeghi, "Surface leakage reduction in narrow band gap type-II antimonide-based superlattice photodiodes", *Appl. Phys. Lett.* **94**, 053506, (2009).
- [4] David Z.-Y. Ting, Cory J. Hill, Alexander Soibel, Sam A. Keo, Jason M. Mumolo, Jean Nguyen, and Sarath D. Gunapala, "A high-performance long wavelength superlattice complementary barrier infrared detector", *Appl. Phys. Lett.* **95**, 023508, (2009)
- [5] J. W. McNabb, H. G. Craighead, H. Temkin, and R. A. Logan, "Anisotropic reactive ion etching of InP in methane/hydrogen based plasmas", J. Vac. Sci. Technol. B 9 (6), 3535, (1991).
- [6] James Werking, Jeff Schramm, Chanh Nguyen, Evelyn L. Hu, and Herbert Kroemer, "Methane/hydrogen-based reactive ion etching of InAs, InP, GaAs, and GaSb", Appl. Phys. Lett. 58, 2003, (1991).
- [7] Andrew Hood, Pierre-Yves Delaunay, Darin Hoffman, Binh-Minh Nguyen, Yajun Wei, and Manijeh Razeghi, "Near bulk-limited R₀A of long-wavelength infrared type-II InAs/GaSb superlattice photodiodes with polymide surface passivation", *Appl. Phys. Lett.* **90**, 233513, (2007).
- [8] Yiqiao Chen, Aaron Moy, Shangheng Xin, Kan Mi, and Peter P. Chow, "Improvement of R₀A product of type-II InAs/GaSb superlattice MWIR/LWIR photodiodes", *Infrared Phys. Technol.* **52**(6), 340-343, (2009).
- [9] B.-T. Lee, T. R. Hayes, P. M. Thomas, R. Pawelek, and P. F. Sciortino Jr., "SiO₂ mask erosion and sidewall composition during CH₄/H₂ reactive ion etching of InGaAsP/InP", *Appl. Phys. Lett.* **63**, 3170, (1993).
- [10] A. Baca and C. Ashby, *Fabrication of GaAs Devices*, The Institution of Engineering and Technology, London, 2005.
- [11] Sir B. Rafol, A. Soibel, A. Khoshakhlagh, J. Nguyen, J. K. Liu, J. M. Mumolo, S. A. Keo, L. Hoeglund, D. Z. Ting, and S. D. Gunapala, "Performance of a ¼ VGA Format Long-Wavelength Infrared Antimonide Based Superlattice Focal Plane Array", to be published in IEEE J. Quant. Electron., (2012).